Attorney's Docket No.: 10559-292001/P9299-ADI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ravi P. Singh et al. Art Unit: 2185
Serial No.: 09/675,569 Examiner: Midys Rojas
Filed: September 29, 2000
Title: A FIFO WRITE/LIFO READ TRACE BUFFER WITH SOFTWARE AND HARDWARE LOOP COMPRESSION

Commissioner for Patents
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to United States Patent and Trademark Office OG Notices: 12 July 2005 - New Pre-Appeal Brief Conference Pilot Program, a request for a review of an initial matter is hereby submitted with the Notice of Appeal. Review of this matter by a panel of examiners is requested because the rejections are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections. The right to address additional matters in any subsequent appeal brief is reserved.

In the action mailed January 17, 2006, independent claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 6,094,729 to Mann (hereinafter "Mann"), U.S. Patent No. 5,553,010 to Tanihara et al. (hereinafter "Tanihara"), and U.S. Patent Publication No. 2003/0115424 to Bachand et al. (hereinafter "Bachand"). Independent claims 18 and 27 were

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rejected under 35 U.S.C. § 103(a) as obvious over Mann and Tanihara.

Applicants traverse these rejections on several grounds. However, for the sake of limiting issues before the panel, Applicants requests that the panel review be limited to the following issue:

1. Does the combination of Mann and Bachand, with or without Tanihara, support a *prima facie* case of obviousness of the comparison of fetched instruction addresses, as recited in claims 1, 18, and 27?

The subject matter of independent claims 1, 18, and 27 relates to trace compression systems and techniques in which fetched instruction addresses are compared. For example, claim 18, which is illustrative, relates to a method that includes a trace operation and a compression operation. The trace operation includes storing an address pair corresponding to a loop in fetched instructions. The compression operation includes comparing the stored address pair to a new address pair in fetched instructions. Thus, each of the compared address pairs are both *fetched instruction addresses*.

None of the cited references involve the comparison of fetched instruction addresses for any reason, much less in the context of trace operation and/or compression as recited in present claims 1, 18, and 27.

For example, Mann, which is the only cited reference that involves trace compression, describes that trace compression is to be achieved on the basis of disruptions to the program flow. *See Mann*, col. 18, line 19-20. Mann's reported instructions are those in which the target address is data dependent. Such reporting does not include every call or branch. *See, e.g., Mann*, col. 18, line 20-25, col. 18, line 28-31, col. 18, line 33-35, col. 18, line 37-38, and col. 18, line 28-31. As a

result of this screening, few of Mann's trace entries contain address values. *See, e.g., Mann*, col. 19, line 21. Thus, Mann's trace compression technique intentionally discards at least some of the addresses that are compared in the subject matter of the present claims and relies upon identifying disruptions to the program flow, rather than a comparison of fetched instruction addresses, to compress traces.

Despite Mann's alternative basis of trace compression and discarding of at least some of the fetched instruction addresses, the rejections contend that Mann can still serve as the basis of an obviousness rejection. This basis for this contention is that a comparison of fetched instruction addresses in Mann is not completely foreclosed. Applicant believes that this contention mistates the obviousness standard and that it neglects the impact of Mann's teachings on one of ordinary skill.

Moreover, even if the express teachings of Mann were to be ignored, a combination of Mann, Bachand, and Tanihara would still not arrive at the claimed subject matter. In this regard, Bachand is directed toward maintaining cache coherency in a multi-agent architecture. A cache is coherent when each agent uses the most current copy of *data* available to the system. *See Bachand*, para. [0003].

Each of Bachand's agents exchanges cache coherency messages (i.e., snoop responses) that identify whether other agents possess copies of requested data in the MESI scheme. *See Bachand*, para. [0009]. For the MESI scheme to operate, these cache coherency messages must be exchanged *before* the data is provided to a requesting agent, lest copies of data that are not current be used. *See Bachand*, para. [0009].

Bachand explicitly states this point in the description of his technology. In particular, in Bachand's system, an external transaction queue compares the address of *newly requested data* with addresses of pending posted transaction data (i.e., transactions with addresses that have not yet been globally observed). *See Bachand*, para. [0025].

Applicant submits that Bachand's newly requested data address is not a fetched instruction address, as recited. To begin with, the MESI scheme is designed to operate with data, not instructions. Further, Bachand is explicit in that any existing possession of data must be identified before another agent can establish possession. To contend otherwise (i.e., that Bachand's comparisons can be made after data is provided to agents), would render the entire MESI scheme inoperable to prevent cache incoherency. Bachand's comparison must therefore occur before data is provided to a requesting agent.

When this deficiency in Bachand was pointed out in the response filed Sept. 30, 2005, the rejection is understood to contend that Bachand's new data requests constitute a fetch command. *See January 17, 2006 Office action*, page 3. However, claims 1, 18, and 27 deal with the comparison of fetched instruction addresses, not new data requests.

Since Bachand's comparisons of data addresses must occur before access is provided, Bachand neither describes nor suggests the comparison of fetched instruction addresses for any reason, much less for trace operation and/or compression as recited in present claims 1, 18, and 27. Bachand therefore does not remedy the above-noted deficiencies with Mann.

Tanihara, which was recited in rejecting claim 1, describes a data shifting circuit of a central processor and has nothing to do with either trace buffer circuits or trace operations. Tanihara thus also does nothing to remedy these deficiencies.

Thus, a clear factual basis for why a *prima facie* case of obviousness of claims 1, 18, and 27 has not been established has been set forth and this issue is ripe for panel review. Further, in light of this basis, claims 1, 18, 27, and the claims dependent therefrom are patentable over Mann, Bachand, and Tanihara in any combination.

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Respectfully submitted,

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